TC9306F

DTS MICRO CONTROLLER CONTAINING LCD DRIVER

The TC9306F is 4 bit CMOS micro controller for digital tuning system use having built-in LCD driver.

CPU has 4 bit parallel addition and subtraction (AI, SI instructions, etc.), logical operation (OR, AN instructions, etc.), plural bit judge and comparison instruction (TM, SL instructions, etc.), and timer function.

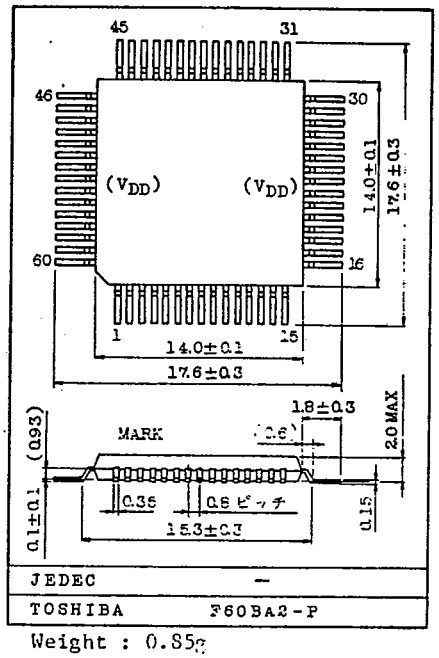
The equipment consists of 60 pin, mini-flat package, and has abundant I/O port and exclusive key input port controlled by powerful input and output instruction (IO, KEY instruction, etc.), and serial bus control function (SIO instruction) to control forcibly external PLL LSI and peripheral ICs.

Further, it contains 4 bit A/D converter, and is capable of measuring electric field strength by inputting signal meter output.

Also, it has abundant exclusive LCD output terminal of 1/2 duty, 1/2 bias driving, and exclusive terminal to output ten kinds of reference frequency signal to be supplied to PLL LSI.

And TC9306F is pin-compatible with TC9302AF (program memory capacity, 1K-step type).

Unit in mm



Weight : 0.85g

FEATURES:

- 4 bit micro controller for digital tuning system use.
- Built-in LCD driver (1/2 duty, 1/2 bias driving, driving frequency: 50Hz)
- 5V±10% single power supply. CMOS structure and low power dissipation.
- Back-up of data memory (RAM) and each port is easily made (by $\overline{INH}$ terminal).
- Program memroy (ROM) : 16 bit × 2048 steps
- Data memory (RAM) : 4 bit × 256 words
- Powerful instruction set of 65 kinds (all one word instruction).
- Instruction executing time 44.4μs (7.2MHz crystal connection).

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- Abundant addition and subtraction instructions (addition instructions 12 kinds, subtraction instructions 12 kinds).
- Powerful compound judge statement (TMTR,TMFR,TMT,TMF,TMIN,TMFN instructions).
- Data transfer in same low address is possible.
- Indirect transfer of register is possible. (MVRD,MVRS,MVGD, MVGS instructions).
- 16 powerful general registers (arranged in RAM).
- Stack level : 2 level
- Program memory (ROM) has no conception of page, field, and JUMP and CAL instruction can be freely made among 2048 steps.
- It is possible to freely refer to the content, 16 bits, of optional address within 1024 steps in program memory (ROM), (DAL instruction).
- Contains powerful exclusive serial bus control function.
- Powerful input and output instruction (IO, KEY, SIO instructions).
- Exclusive input port (K_0~K_3) for key input use, and abundant 29 exclusive LCD driving terminals.
- Abundant 14 I/O port (port capable of setting input or output in 1 bit unit : 6, exclusive output port : 8).
- Clock stop is possible by instruction. (During CKSTP instruction : Supply current, 1μA or below).
- 2Hz timer F/F and 10Hz interval pulse output are contained (Internal port for time base use).
- Built-in 4 bit A/D converter
- Reference frequencies of ten kinds to be supplies to PLL LSI can be selected depending upon program. (1kHz, 5kHz, 9kHz, 10kHz, 12.5kHz, 25kHz, 50kHz, 100kHz, 3.125kHz, 6.25kHz).
- Pin-compatible with TC9302AF (ROM capacity: 16-bit × 1024 steps).

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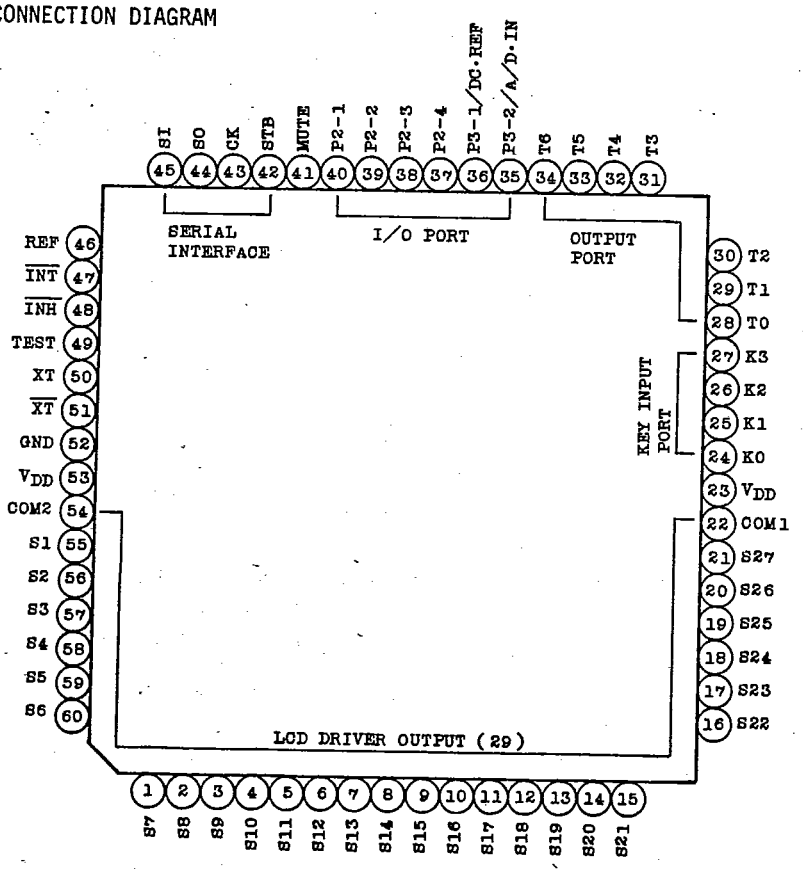
MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	-0.3~6.0	V
Input Voltage	V_{IN}	-0.3~V_{DD}+0.3	V
Power Dissipation	P_D	200	mW
Operating Temperature	Topr	-30~75	°C
Storage Temperature	Tstg	-55~125	°C

TERMINAL CONNECTION DIAGRAM



TOP VIEW MINI FP-60PIN

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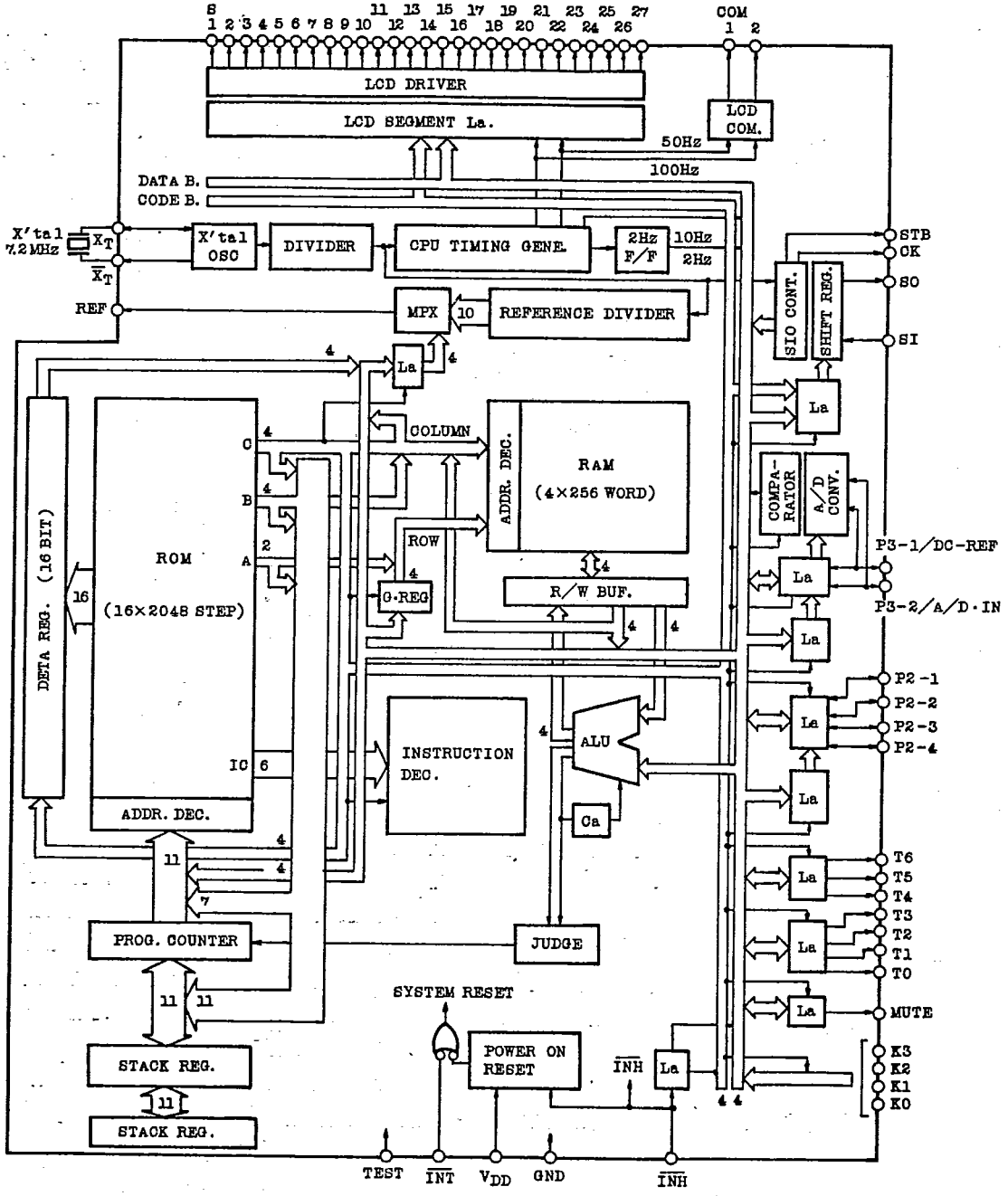
BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta=25°C, V_{DD}=5V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage Range	V_{DD}	*	4.5	5.0	5.5	V
Memory Holding Voltage Range	V_{HD}	Crystal oscillation stops *	2.0	~	5.5	V
Operating Supply Current	I_{DD}	Normal operation (Encluding output current)	-	1.0	3.0	mA
Memory Holding Supply Current	I_{HD1}	V_{DD}=5V Crystal oscillation stops	-	0.07	1.0	μA
	I_{HD2}	V_{DD}=2V Crystal oscillation stops	-	-	0.5	
Crystal Oscillation Frequency	f_{XT}	*	-	7.2	-	MHz
LCD Common Output (COM1, COM2)						
High Level Output Current	I_{OH1}	V_{OH}=4.5V	-200	-500	-	μA
Low Level Output Current	I_{OL1}	V_{OL}=0.5V	200	500	-	μA
1/2 Bias Voltage	V_{BS}		2.40	2.50	2.60	V
LCD Segment Output (S1~S27)						
High Level Output Current	I_{OH2}	V_{OH}=4.5V	-50	-160	-	μA
Low Level Output Current	I_{OL2}	V_{OL}=0.5V	50	160	-	μA
MUTE, T0~T6 Port						
High Level Output Current	I_{OH3}	V_{OH}=4.5V	-0.7	-1.7	-	mA
Low Level Output Current	I_{OL3}	V_{OL}=0.5V	0.5	1.2	-	mA
REF Output, P2-1~-4, P3-1~-2 Port						
High Level Output Current	I_{OH4}	V_{OH}=4.0V	-0.6	-1.4	-	mA
Low Level Output Current	I_{OL4}	V_{OL}=1.0V	0.6	1.4	-	mA
SO, CK, STB Output						
High Level Output Current	I_{OH5}	V_{OH}=4.0V	-1.0	-2.0	-	mA
Low Level Output Current	I_{OL5}	V_{OL}=1.0V	1.0	2.0	-	mA
Key Input Port (K0~K3)						
High Level Input Voltage	V_{IH1}		3.5	~	5.0	V
Low Level Input Voltage	V_{IL1}		0	~	1.5	V
Pulldown Resistance	R_{IN1}		50	100	150	kΩ

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ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta=25°C, V_{DD}=5V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
SI, $\overline{INH}$, $\overline{INT}$, P2-1~4, P3-1~2 Port						
High Level Input Voltage ($\overline{INH}$)	V_{IH2}		4.3	~	5.0	V
Low Level Input Voltage ($\overline{INH}$)	V_{IL2}		0	~	2.7	V
High Level Input Voltage (Others)	V_{IH1}		3.5	~	5.0	V
Low Level Input Voltage (Others)	V_{IL1}		0	~	1.5	V
High Level Input Leak Current	I_{IH}	V_{IH}=5.0V	-	-	1.0	μA
Low Level Input Leak Current	I_{IL}	V_{IL}=0V	-	-	-1.0	μA
A/D Converter (DC·REF, A/D IN)						
DC·REF Built-in Ladder Resistance	$\overline{RL}$		30	50	80	kΩ
DC·REF Input Voltage Range	V_{REF}		1.0	~	3.0	V
Resolution	V_{RES}		-	V_{REF} /16	-	V
Others						
XT Input Feedback Resistance	Rf		500	1000	2000	kΩ
Test Input Pulldown Resistance	R_{IN2}		15	30	60	kΩ

Note: * Marked items are guaranteed within a range of V_{DD}=4.5~5.5V, Ta=-30~75°C.

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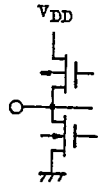
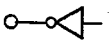
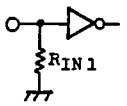
FUNCTIONS OF EACH TERMINAL

PIN No.	SYMBOL	TERMINAL NAME	FUNCTION AND OPERATION	REMARKS
22 54	COM1 COM2	LCD Common Output	This is a common signal output terminal to LCD. Indication of maximum 54 segments is possible with matrix made with S1~S27. To this terminal are outputted three value levels of V_{DD}, 1/2V_{DD}, GND, at intervals of 50Hz. (Note) During system reset and CKSTP instruction execution, output is automatically fixed at "L" level.	
55 〜 60 1 〜 21	S1 〜 S6 S7 〜 S27	LCD Segment Output	This is a segment signal output terminal to LCD. Indication of maximum 54 segments is possible with matrix mode with COM1, COM2. Data is outputted to these terminals by the execution of SEG instruction (COM1 system) and MARK instruction (COM2 system). Decoding of segment can be done by making that decode pattern within ROM territory and executing it by using DAL instruction. (Note) During system reset and CKSTP instruction execution, output is automatically fixed at "L" level.	
24 〜 27	K0 〜 K3	Key Input Port	This is a 4 bit input port for inputting key matrix. By executing KEY instruction designating this port at operand part, data of these terminals is read in RAM. All terminals contain pull-down resistance. Usually, output port of T0~T6 is used for key return timing signal output.	

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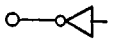
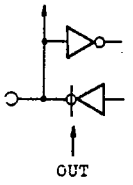
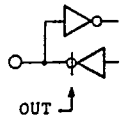
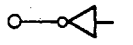
FUNCTIONS OF EACH TERMINAL

PIN No.	SYMBOL	TERMINAL NAME	FUNCTION AND OPERATION	REMARKS
28 ~ 34	T0 ~ T6	Key Timing Output Port	This is an output port of 4 bit (T0~T3) and 3 bit (T4~T6). Usually, it is used as key return timing signal output of key matrix.	
35	P3-2 /A/D. IN	I/O Port 3 A-D/Analog Voltage Input /Reference Voltage Input	This is a 2 bit I/O port. This port is capable of making input and output assignment for each bit, and the assignment is made with the content of internal port called PORT-3 I/O CONTROL. This terminal combines analog input of built-in 4 bit A/D Converter. Change-over to A/D Converter input is also controlled by the content of PORT-3 I/O CONTROL Port. The built-in A/D converter is of successive comparison system by program, P3-1 being reference voltage input, and P3-2 analog comparison voltage input.	To A/D Converter 
36	P3-1 /DC. REF			
37 ~ 40	P2-4 ~ P2-1	I/O Port 2	This is a 4 bit I/O port. This port is capable of designating input and output of each bit, and the designation is performed with the content of internal port called PORT-2 I/O CONTROL.	
41	MUTE	Muting Signal Output Port	This is a 1 bit output port. It is usually used as a muting control signal output.	

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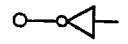
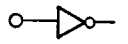
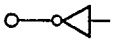
FUNCTIONS OF EACH TERMINAL

PIN No.	SYMBOL	TERMINAL NAME	FUNCTION AND OPERATION	REMARKS
42	STB	Strobe Pulse Output	Serial interface. By executing SIO instruction, external PLL LSI and peripheral optional ICs can be controlled powerfully. As for serial transfer system, two kinds of $\overline{\text{NCD}}$/NCD mode can be selected by program.	
43	CK	Serial Clock Output		
44	SO	Serial Data Output		
45	SI	Serial Data Input		
46	REF	Reference Frequency Signal Output	This is an output terminal of reference frequency signal supplied to PLL LSI. It is possible to select ten kinds of reference frequency signal, 1kHz, 5kHz, 9kHz, 10kHz, 12.5kHz, 25kHz, 50kHz, 100kHz, 3.125kHz, 6.25kHz, depending upon the program. (Note) When $\overline{\text{INH}}$ input is at "L" level, output is automatically fixed at "L" level.	
47	$\overline{\text{INT}}$	Initializing Input	This is a system reset signal input terminal of the device. While $\overline{\text{INT}}$ is at "L" level, reset is applied, and when it becomes "H" level, the program starts from zero address. When the voltage, 0V→4.5V, is supplied to V_{DD} terminal, system reset is applied (power on reset), and so this terminal usually is fixed at "H" level when used. (Note) After system reset, I/O port is set at input mode, but the output port must be initialized by program according to your use, as its output condition is indefinite.	

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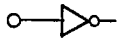
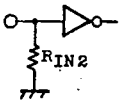
PIN No.	SYMBOL	TERMINAL NAME	FUNCTION AND OPERATION	REMARKS
48	$\overline{INH}$	Inhibit Input	This is a pulsing signal input port of radio mode. It judges as radio on mode at "H" level input and radio off mode at "L" level input. When this terminal is at "L" level, REF output is automatically fixed at "L" level. Further, if CKSTP instruction is used in the program and this CKSTP instruction is executed while $\overline{INH}$ is at "L" level, the internal clock generator and CPU stop their operations, and memory back up condition can be realized at low current consumption (less than 1μA). At this time, all output terminals (display output, output port, etc.) are fixed to "L" level, automatically. (Note) CKSTP instruction is effective when $\overline{INH}$ is at "L" level, and makes the same operation as NOOP instruction if executed when $\overline{INH}$ is at "H" level.	
49	TEST	Test Mode Control Input	This is an input terminal for a test mode control. It is brought to test mode with "H" level input and normal operation with "L" level or NC condition. It contains pull down resistance, and usually fixed at NC or "L" level when used. In the test mode, the device operates as evaluator chip, and program evaluation at EPROM base is possible when combined with external simulation board.	

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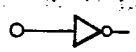
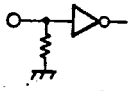
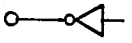
FUNCTIONS OF EACH TERMINAL

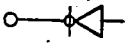
PIN No.	SYMBOL	TERMINAL NAME	FUNCTION AND OPERATION	REMARKS
50 51	XT $\overline{XT}$	Crystal Oscillation Terminal	This is a connecting terminal of crystal resonator. 7.2MHz crystal is connected. Oscillation is automatically stopped during the execution of CKSTP instruction.	-
52	GND	Ground Terminal	This is a device ground terminal.	-
23 53	V_{DD}	Power Supply Terminal	This is a power supply terminal of the device. Voltage of 5V±10% is impressed in the normal operation. Under back up condition (during the execution of CKSTP instruction), voltage can be lowered down to 2V. When voltage, 0V→4.5V, is supplied to this terminal, system reset is applied to the device, and the program starts from zero address. (power on reset). (Note) Carry out power on reset from the condition of $\overline{INH}$="L" level. (Note) As the content of each port (output port, internal port, etc.) is indefinite at the time of closing of supply power, initialization by program must be made, according to your use.	-

(Supplement)


CMOS input


Built-in pulldown resistance CMOS input


CMOS output


Clocked gate type CMOS output